Amendments to the Specification:

Please replace the paragraph beginning on page 12, line 23 with the following amended paragraph:

--Figure 5 illustrates an enlarged detailed view of a memory area from Figure 2. Bit lines 1 can run divergently with respect to one another and can be crossed by curved second lines 2, as in Figure 4. Mutually adjacent first lines, for example, bit lines BL10, BL11, can enclose an angle W, which is smaller than in Figure 4, since the capacitors 3 can be arranged to be compressed by lateral offsets along the curved lines 2, for example, the word lines WL1 to WL4. Hence, the arcuately running word lines can also make contact with a relatively large number of memory cells on a relatively short annular circumference or arcuate section, which means that the signal delays along the second lines are relatively homogeneous.--

Please replace the paragraph beginning on page 13, line 7 with the following amended paragraph:

-- The interconnection of the memory cells can be different in Figures 4 and 5. Each word line 2 in Figure 5 can be connected to two rows of memory cells 5, which can curved concentrically with respect to the word line. The memory cells 3 can be connected to a respective single word line 2 can be arranged in the form of a zigzag line to be offset alternately above and below the word line in Figure 5, i.e., offset with respect to the word line 2 on the left and right thereof in relation to the substrate surface. As a result, one word line can actuate more memory cells per word line length than in the case of a conventional semiconductor memory. In a conventional semiconductor memory, two memory cells 5a, which can be connected to the same bit line BL11 and [[cam]] can be adjacent to one another along this bit line BL11, can be connected to different word lines 2, which are most closely adjacent to one another, in figure 5 too, which means that the inventive semiconductor memory can be used for actuating just a single memory cell in each case. The storage capacitors for the memory cells 5a can be connected to a particular single bit line and can be arranged to be offset either on the right or on the left of the word line, which is connected to them.--